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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JENSEN HARTRUNG JENSEN

Appeal 2009-004494
Application 10/052,277[1]
Technology Center 2100

Decided: December 9, 2009

Before JEAN R. HOMERE, STEPHEN C. SIU and
DEBRA K. STEPHENS, *Administrative Patent Judges.*

HOMERE, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] Filed on January 17, 2002. The real party in interest is NXP B.V.

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 (a) from the Examiner's final rejection of claims 1 through 8, 10 through 13, and 15 through 19. Claims 9 and 14 have been canceled. We have jurisdiction under 35 U.S.C. § 6 (b).

We affirm.

Appellant's Invention

Appellant invented a method and system for reducing the amount of power consumed in a bus interface structure to thereby produce a low power consuming bus architecture that operates at high speed with minimal data transfer latency. (Spec. 2, [para. 0005].) As shown in Figure 1, the bus architecture (100) includes a plurality of initiators (110) coupled to a bus controller (150) via respective first interface adapters (115). The bus controller (15) is subsequently coupled to a plurality of targets (120) via respective second interface adapters (125) such that any of the initiators (110) can communicate with any of the targets (120). (Spec. 3, [para. 0011].) The bus architecture (100) further includes an activity detector (180) that, upon being notified that the initiator (110) has initiated a data transfer process, communicates an enabling signal to the target devices interfaces (125) allowing them to receive the transferred data. (*Id.* [para. 0012, 0014].) Subsequently, upon being notified that the data transfer process is complete, the activity detector (180) terminates the enabling signal and issues an inhibit signal to inhibit the propagation of the system clock to each of the target devices interfaces (125), thereby reducing power consumption therein. (Spec. 4, [para. 0015].)

Illustrative Claim

Claims 1 and 2 further illustrate the invention. They read as follows:

> 1. A system comprising: a plurality of components, a bus structure that is configured to facilitate communications among the plurality of components, and an activity detector that is configured to detect an initiation of a data- transfer operation and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of said components, wherein the bus interface is configured to be enabled to receive data from the bus structure as part of said data-transfer operation upon receipt of the enabling signal from the activity detector.
>
> 2. The system of claim 1, wherein the activity detector is further configured to detect a completion of the data-transfer operation, and terminates the enabling signal based on the completion of the data-transfer operation, and the bus interface is configured to be disabled from receiving data from the bus structure upon termination of the enabling signal.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Mitchell	5,987,614	Nov. 16, 1999

Rejection on Appeal

The Examiner rejects the claims on appeal as follows:

Claims 1 through 8, 10 through 13, and 15 through 19 stand rejected as being anticipated by Mitchell.

Appellant's Contentions

Appellant contends that Mitchell does not teach an enabling signal that is communicated to bus interfaces of a plurality of components, as recited in independent claim 1. (App. Br. 8, Reply Br. 2.) According to Appellant, Mitchell discloses providing a separate signal to each of a plurality of bus interfaces, whereas the claim requires providing the same enabling signal to all the interfaces of the components upon an activity detector receiving an indication that an initiator has initiated a data transfer operation. (App. Br. 8-9.) Further, Appellant expresses doubts regarding whether Mitchell's activity monitor actually detects initiation of a data transfer operation since the different power management states (DOZE, SLEEP, SUSPEND, etc.) in Mitchell are set by a software running on a CPU. (Reply Br. 2-3.)

Examiner's Findings

The Examiner finds that Mitchell's disclosure of integrating a conventional central power management unit (PMU) in a power management system teaches a unit that monitors activities on a bus to send an operating signal (e.g. ON, DOZE, SLEEP, OFF) to a plurality of bus interfaces of a respective plurality of components to alter the states of said components upon detecting a data transfer activity on the bus. (Ans. 8-12.)

II. ISSUE

Has Appellant shown that the Examiner erred in finding that Mitchell teaches providing an enabling signal to a plurality of bus interfaces of a respective plurality of components upon an activity detector receiving an

indication that an initiator has initiated a data transfer operation, as recited in independent claim 1?

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Mitchell

1. As shown in Figure 1, Mitchell discloses a system for reducing power consumption in a computer system (10) having a plurality of buses (26, 27, 28) coupled to a plurality of components (31-36) via respective bus interfaces. (Abstract; col. 1, ll. 32-42.)

2. Mitchell discloses integrating a PMU (20) in the power management system, wherein the PMU (20) includes an activity monitor (21) that passively watches activities of system resources on the bus (e.g. access to ports for reading or writing data). (Col. 1, ll. 32-43; col. 6, ll. 47-50.)

3. Mitchell discloses upon receiving an indication that one of the devices is initiating a data access, the activity monitor (21) issues a signal (ON, DOZE, OFF, SLEEP, or SUSPEND) to each interface of the plurality of components to thereby alter the operating state of such components in order to reduce power consumption therein. (Col. 1, ll. 43-56; col. 2, ll. 11-19.)

IV. PRINCIPLES OF LAW

Anticipation

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992)).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (citation omitted.) "In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art." *Id.*

V. CLAIM GROUPING

Appellant argues the patentability of claim 1 in conjunction with the rejection of claims 1 through 8, 10 through 13, and 15 through 19.[2] In

[2] Appellant presents separate arguments for claims 2, 5, 6, 10 through 11, 15 through 19. (Reply Br. 3-4.) First, we note that such arguments were not raised in the Appeal Brief, and they are not presented for the first time in the Reply Brief in response to new arguments raised in the Examiner's Answer. Therefore, these arguments are waived since they were not timely raised. *See Optivus Tech., Inc. v. Ion Beam Applications S.A.*, 469 F.3d 978, 989(Fed. Cir. 2006) (an issue not raised in an opening brief is waived). *See Becton Dickinson and Co. v. C.R. Bard, Inc.*, 922 F.2d 792, 800 (Fed. Cir. 1990.) Second, we note that the cited arguments merely repeat the language

accordance with 37 C.F.R. § 41.37 (c) (1) (vii), we will consider all the claims on appeal as standing and falling with representative claim 1.

VI. ANALYSIS

Independent claim 1 requires in relevant part providing an enabling signal to a plurality of bus interfaces of a respective plurality of components upon an activity detector receiving an indication that an initiator has initiated a data transfer operation.

As set forth in the Findings of Fact section, Mitchell discloses an activity monitor in a power management system that issues a signal to the interfaces of a plurality of components to thereby alter the operating states of the components upon being notified that one of said components has initiated a data access request to write or read data. (FF. 1-3.) We find that by issuing a request to access a component to write data thereto or read data therefrom, Mitchell teaches that such request is made for the purpose of transferring data to or from the component desired to be accessed. Further, we find that by altering the operating state of each of the component interfaces in response to detecting the transfer of data was initiated by one of the components, Mitchell teaches sending a signal (ON, DOZE, OFF, SLEEP, or SUSPEND) to enable the interface of each of the plurality of components to allow the transfer of data to take place among the components. We therefore agree with the Examiner that Mitchell's power management system as depicted in Figure 1 teaches the invention, as recited

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of the claims, and generally allege patentability over the prior art without showing how the cited claim language is patentably distinguishable over the cited prior art. They therefore do not constitute separate arguments. Consequently, we will not consider these arguments in this Opinion.

in claim 1. It follows that Appellant has not shown that the Examiner erred in finding that Mitchell anticipates claim 1.

VII. CONCLUSION OF LAW

Appellant has not established that the Examiner erred in rejecting claims 1 through 8, 10 through 13, and 15 through 19 as being anticipated under 35 U.S.C. § 102(b).

VIII. DECISION

We affirm the Examiner's rejection of claims 1 through 8, 10 through 13, and 15 through 19.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136 (a) (1) (iv).

AFFIRMED

llw/nhl

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